

Introduction to the UTMI+ Low Pin Interface (ULPI)

As new technologies emerge, they allow us to design smarter, faster, and smaller peripherals. To address the increasing popularity of the portable market, the On-The-Go Supplement to the USB 2.0 Specification was developed. USB is poised to dominate the portable market as the high-speed connection of choice. Just look at the advantages that USB and On-The-Go have to offer:

- A household name with more than 1.4 billion USB enabled PC's and peripherals shipped worldwide.
- A thorough compliance and logo program operated by the USB-IF. This guarantees a smooth and trouble-free experience for the user.
- A large group of industry vendors offering a plethora of USB solutions, including IP blocks, SoC parts, discrete chips, software drivers and systems.
- Provides flexibility based on system needs. Bus speed and device complexity can be configured at design time.
- On-The-Go devices do not require a PC host, and can communicate directly with each other. As an example, Figure 1 shows a Dual-Role PDA that can perform as a USB host and print directly to a USB printer, and also act as a USB peripheral to communicate with a PC.

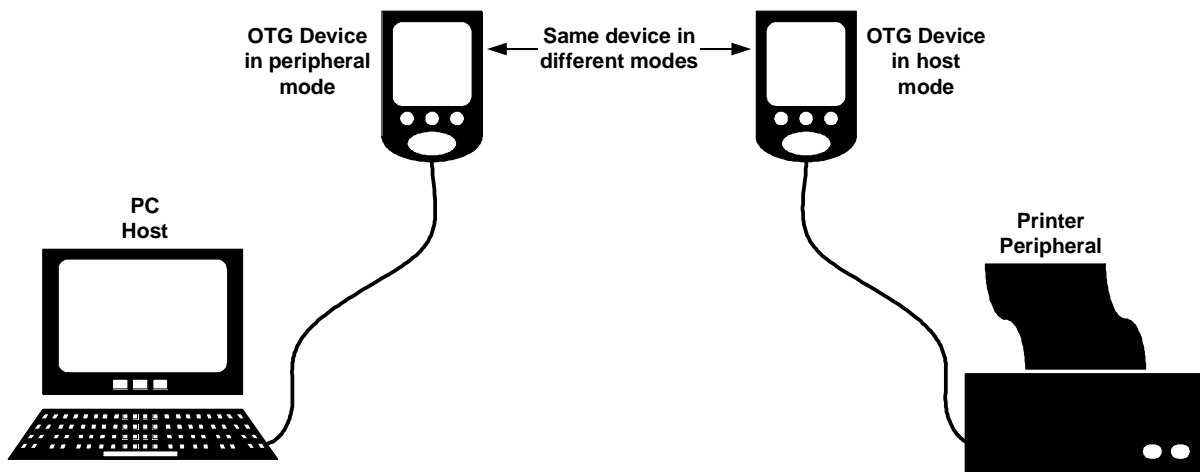


Figure 1 – An On-The-Go Device can act as host and/or peripheral

Designers all over the world are faced with increasing pressure to design smaller products, in less time, and at lower cost. At the same time, as smaller deep sub-micron processes are introduced, integrating the physical layer analog circuitry required by technologies such as USB and On-The-Go is a task that has become a technical challenge, requiring more man-hours, more investment, and more silicon spins.

To get a product to market faster while keeping costs low, the physical layer can be provided in a separate chip. The designer integrates the bulk of the USB digital logic into the ASIC in a very fast time, and connects it to an external PHY that is proven and already available on the market.

Announced on March 1, 2004, the ULPI specification provides a low-pin, low-cost, small form-factor transceiver interface for any USB application.

ULPI was developed by a group of USB industry leaders to address the need for low-cost USB and OTG PHYs. Existing specifications including UTMI and UTMI+ were developed primarily for Macrocell (IP) development, and are not optimized for use as an external PHY. Using the existing UTMI+ specification as a starting point, the ULPI working group reduced the number of interface signals to 12 pins, with an optional implementation of 8 pins. The package size of PHY and Link IC's are drastically reduced. This not only lowers the cost of Link and PHY IC's, but also makes for a smaller PCB.

Benefits of ULPI

- Proven interface.
- Non-proprietary industry standard.
- Minimizes pin count, cost and board space for USB host, peripheral and OTG applications.
- Compatible with USB 1.1, USB 2.0, UTMI, UTMI+, OTG, and LPM.
- Supports USB High Speed (480Mbit/s), Full Speed (12Mbit/s), and Low Speed (1.5 Mbit/s).
- Allows reuse of existing UTMI and UTMI+ Link and PHY designs.
- Compliant IP and discrete IC's are available from multiple sources.

Acronyms and Terms

A-device	Device with Standard-A or Micro-A plug inserted into its receptacle
B-device	Device with Standard-B or Micro-B plug inserted into its receptacle
DRD	Dual-Role Device
EOP	End-Of-Packet pattern
FS	Full Speed
HNP	Host Negotiation Protocol
IP	Intellectual Property
Link	ASIC, SIE, or FPGA that connects to the ULPI PHY
LPM	Link Power Management
LS	Low Speed
NRZI	Non-Return to Zero Inverted encoding
OTG	On-The-Go
PC	Personal Computer
PDA	Personal Digital Assistant
PHY	Physical Layer (Transceiver)
PID	Packet Identifier
SIE	Serial Interface Engine
SoC	System on Chip
SRP	Session Request Protocol
SYNC	Synchronization pattern
T&MT	Transceiver and Macrocell Tester
USB	Universal Serial Bus
USB-IF	USB Implementers Forum
UTMI	USB 2.0 Transceiver Macrocell Interace
UTMI+	UTMI extension supporting USB host and On-The-Go
UUT	Unit Under Test

UTMI Overview

Following the release of the USB specification, Intel released the UTMI specification. UTMI defines an interface between two IP blocks: the USB Transceiver Macrocell (IP) and the USB Link layer (SIE). The UTMI interface provides functionality for USB peripherals only, not for USB hosts or On-The-Go.

The signals for a UTMI interface with an 8-bit bi-directional data bus are depicted in Figure 2. A minimum of 22 signals is required between the Link and PHY. The following extra pins are found on a typical PHY IC package.

- 15-25 pins for power and ground.
- 2 pins for **D+** and **D-** of the USB connector.
- 2 pins for crystal attachment.
- 1-2 pins for stable reference resistor/current source.

This results in a typical PHY package size of 48 to 56 pins. With a 16-bit bi-directional data bus, the package size is typically 56 to 64 pins. Given that a Full Speed PHY IC package is typically 16 pins, the UTMI package size is a prohibitive and costly upgrade to High Speed.

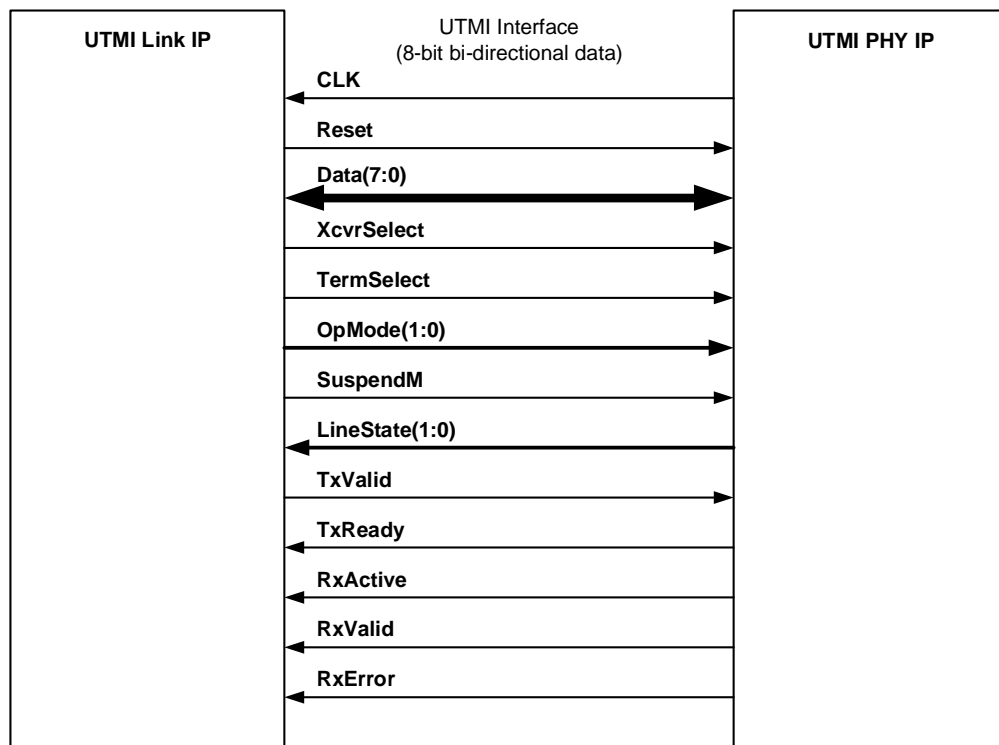


Figure 2 – UTMI interface

The UTMI specification divides USB functionality between the peripheral link and PHY. The PHY contains an analog transceiver and some digital processing logic. Specifically, the PHY provides the following functions for the Link to use.

- Transmits and receives USB data at High Speed (480Mbit/sec), Full Speed (12Mbit/sec), and Low Speed (1.5Mbit/sec).
- Transmits and receives data within the USB requirements of frequency, jitter and duty cycle.
- Serializes 8 or 16-bit parallel data from the SIE for transmission on the USB cable.
- Deserializes data from the USB cable into 8 or 16-bit parallel data.
- Provides flow control for both transmit and receive data, indicating to the Link when new transmit data is needed and when new receive data is ready.
- Inserts stuff bits and performs NRZI encoding for transmit data. Removes stuff bits and performs NRZI decoding for receive data.
- Provides markers for USB packet timing to the Link for bus turnaround and timeout calculations.
- Provides control signals for selection of speed, operational mode, bus resistors, and power settings.
- Is completely under Link control, providing no automatic features. This gives more flexibility in Link design.

The Link layer is the bridge between software and the PHY. The Link must be designed to use the UTMI signals and protocol for all USB operations, including but not limited to the following:

- Control the mode settings of the PHY
- Report USB timeout events to software
- Buffer data during USB receive and transmit
- Format data into transactions
- Control the PHY to perform High Speed Handshake Protocol (Chirp)

Table 1 summarizes how the Link uses UTMI signals. The 16-bit signals [Data(15:8), DataBus16_8, and ValidH] have been omitted because ULPI does not provide a 16-bit implementation option. Similarly, the Vendor Status and Control signals [VControlLoadM, VControl(3:0), and VStatus(7:0)] have been omitted because they are optional debug signals not provided in ULPI.

Please refer to the UTMI specification for more information on UTMI.

Signal Name	Direction on PHY	Signal Description
CLK	OUT	Interface clock. 60MHz for 8-bit implementations. The link uses this clock to synchronously clock data and control signals to/from the PHY.
Reset	IN	Asynchronous reset to all state machines in the PHY. The link typically resets the PHY on power-up only.
Data	I/O	8-bit bi-directional data bus, synchronous with the rising edge of clock . The link can drive the data bus when it drives TXValid high.
XcvrSelect	IN	Transceiver Select. Used by the link to control USB signaling speed. 0 High Speed (480Mbit/s) 1 Full Speed (12Mbit/s)
TermSelect	IN	Termination Select. Used by the link to control USB bus terminations. 0 45Ω terminations connected to D+ and D- (High Speed) 1 1.5kΩ pull-up connected to D+ (Full Speed)
OpMode (1:0)	IN	Operational Mode. Used by the link to control how the PHY drives data onto the USB cable. 00 Normal Operation. The PHY automatically adds SYNC and EOP, inserts stuff bits and NRZI encodes the data. 01 Non-driving. The USB transmitter is disabled. All bus resistors are detached. 10 Disable bit stuffing and NRZI encoding. 11 Reserved.
SuspendM	IN	Active low suspend. Shuts down all logic not needed for suspend/resume.
LineState (1:0)	OUT	USB line status. Used by the link as an accurate representation of the state of the USB D+ and D- lines.
TXValid	IN	Transmit Valid. Asserted by the link to begin transmitting a packet on the USB. De-asserted when the PHY has consumed the last byte.
TXReady	OUT	Transmit Ready. Asserted by the PHY to request the next byte from the link. Used only when TXValid is asserted.
RXActive	OUT	Receive Active. Asserted by the PHY when a SYNC pattern has been detected. De-asserted when an EOP pattern has been detected. Used by the link for receiving data and to calculate High Speed packet timing.
RXValid	OUT	Receive Valid. Asserted by the PHY when the byte on Data contains a valid, decoded USB data byte. Used by the link to clock in data bytes. RXActive must also be asserted for a data byte to be valid.
RXError	OUT	Receive Error. Asserted by the PHY to indicate an error in data received on the USB cable.

Table 1 – Functional summary of UTMI signals

UTMI+ Overview

The UTMI+ specification was developed to address increasing demand for embedded host and On-The-Go capabilities in USB devices. UTMI+ is an extension to the original UTMI specification that defines an interface between two IP blocks: the USB Transceiver Macrocell (IP) and the USB Link layer (SIE), and is not intended to be used as an interface between two discrete chips.

UTMI+ adds host and On-The-Go capabilities to the USB system. Using UTMI as a starting point, UTMI+ incrementally adds new functionality and interface signals to the Link and PHY. Designers can reuse all blocks from their original UTMI IP, and need only add the new circuits required for host or On-The-Go support. This approach works well for UTMI+ because USB peripherals need only a subset of host and On-The-Go functionality.

UTMI+ introduces four levels of functionality, as shown in Figure 3. Each higher level increases the complexity required in both hardware and software, yet is backward compatible with the lower levels.

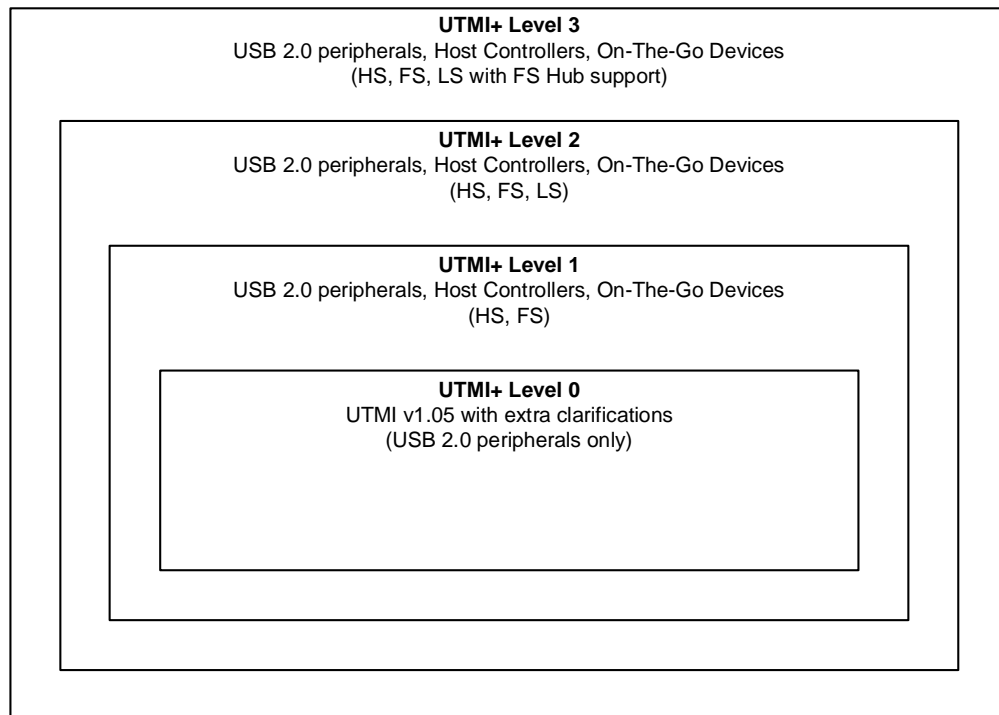


Figure 3 – UTMI+ levels

UTMI+ Level 0

Level 0 is identical to the original UTMI specification, and can be used only for USB peripherals. Several clarifications to the original UTMI specification have also been added based on further industry experience with the practical requirements of a UTMI interface.

This level is recommended for use in applications that require USB peripheral support only.

UTMI+ Level 1

Level 1 adds support for host controllers and OTG devices that need to communicate at Full Speed and High Speed bit rates.

For host support, UTMI+ adds three new features. The first indicates when a peripheral is connected or disconnected. The second provides two 15kΩ bus resistors as host terminations. The third is an optional set of signals for legacy host controller support, including a FS/LS serial interface.

For On-The-Go support, several signals drive and monitor voltage on VBUS. A new circuit is also required to detect which end of the micro-USB cable is plugged in. Note that the OTG specification adds a new ID pin to the micro-USB plug as shown in Figure 4.

This level is recommended for use in applications that require host or OTG functionality operating at Full and High Speed bit rates.

UTMI+ Level 2

Level 2 enables host and OTG devices to support Low Speed traffic. Low Speed peripherals must be attached directly to the PHY port without passing through any hub layer(s). The PHY must be capable of transmitting and receiving USB data at Low Speed bit rates with Low Speed rise and fall times. New analog circuits that support Low Speed operation are usually required in the PHY.

This level is recommended for use in applications that require host or OTG functionality operating at all three bit rates – Low, Full, and High Speed.

UTMI+ Level 3

Level 3 allows host and OTG devices to support Low Speed traffic through a Full Speed hub. The PHY must automatically encase the Low Speed packet with “preamble” markers. Low Speed traffic is sent over the Full Speed bus with Full Speed edge timings at Low Speed bit rates.

This level is recommended for applications that require complete host or OTG support, including Low Speed peripheral and Full Speed hub attachment.



NOTE: Drawings are not indicative of actual plugs, but are to illustrate the ID pin only.

Figure 4 – Standard-USB vs Micro-USB plugs

The signals for a UTMI+ interface with an 8-bit bi-directional data bus are depicted in Figure 5 and described in Table 2. A minimum of 35 signals is required between the Link and PHY. The following extra pins are found on a typical PHY IC package:

- 15-25 pins for power and ground
- 4 pins for **D+**, **D-**, **VBUS**, and **ID** of the USB connector
- 2 pins for crystal attachment
- 1-2 pins for stable reference resistor/current source

This results in a typical PHY package size of 64 to 72 pins. With a 16-bit bi-directional data bus, and including the optional signals, the package size can be 72 to 80 pins. This is prohibitive and costly for use with a single OTG port.

Please refer to the UTMI+ specification for more information on UTMI+.

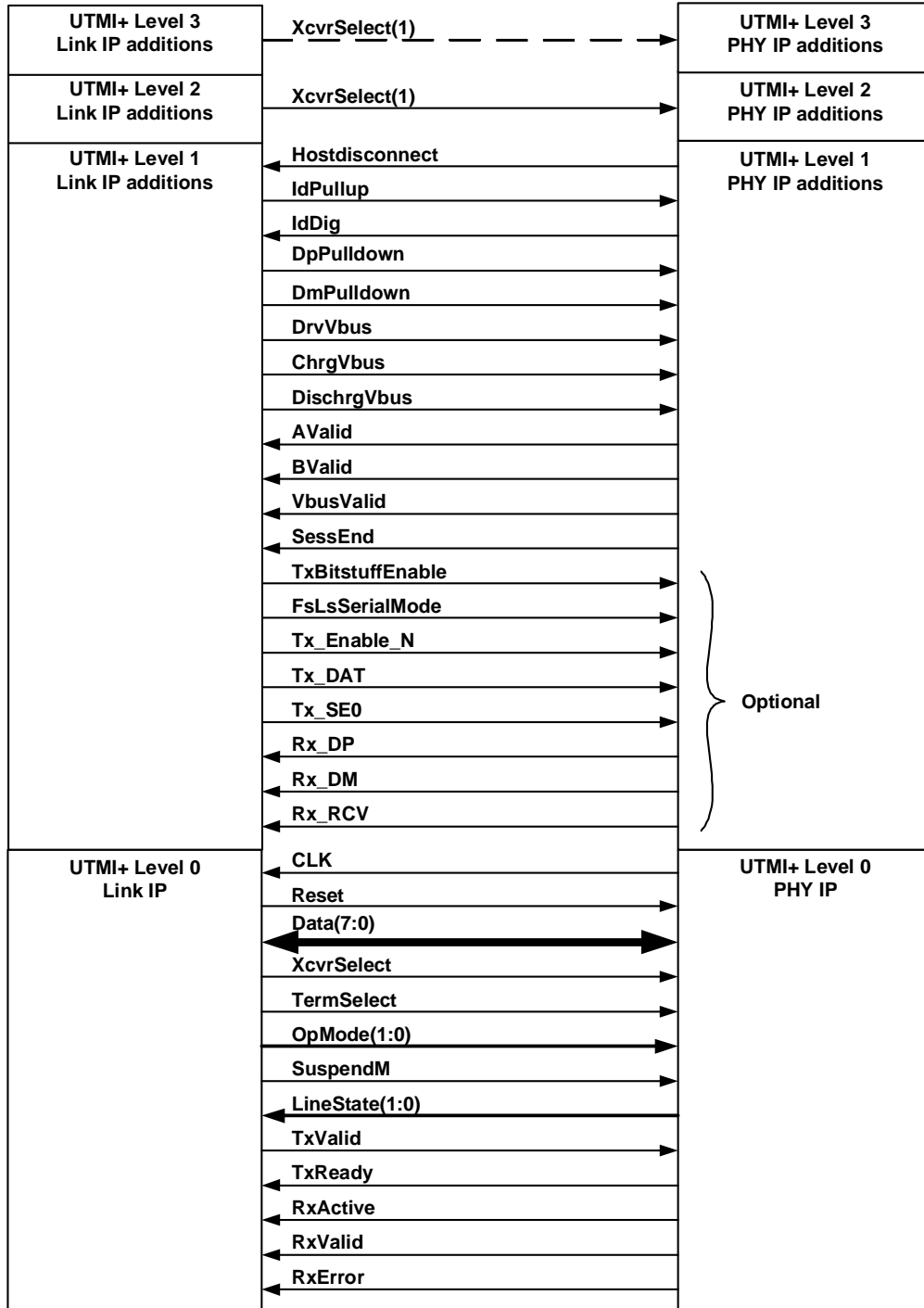


Figure 5 – UTMI+ Level 3 interface

Signal Name	Direction on PHY	Signal Description
<i>Level 0 (No additional signals)</i>		
<i>Level 1</i>		
Hostdisconnect	OUT	Signals to the host if there is a peripheral connected or disconnected.
IdPullup	IN	ID Pull-up. Enables sampling of the ID pin of the USB connector.
IdDig	OUT	ID Digital. Indicates the value of the ID pin of the USB connector.
DpPulldown	IN	Controls the attachment of a 15kΩ resistor on D+ for host termination.
DmPulldown	IN	Controls the attachment of a 15kΩ resistor on D- for host termination.
DrvVbus	IN	Controls the driving of 5V power on VBUS .
ChrgVbus	IN	Controls charging of VBUS for initiating SRP.
DischrgVbus	IN	Controls discharging of VBUS for completing SRP.
AValid	OUT	Indicates if VBUS is above the A-Device session valid threshold. The threshold, V_{th} , is $0.8V \leq V_{th} < 2.0V$.
BValid	OUT	Indicates if VBUS is above the B-Device session valid threshold. The threshold, V_{th} , is $0.8V \leq V_{th} < 4.0V$.
VbusValid	OUT	Indicates if VBUS is above the threshold for normal operation. The threshold, V_{th} , is $4.4V \leq V_{th} < 4.75V$.
SessEnd	OUT	Indicates if VBUS is below the B-Device session end threshold. The threshold, V_{th} , is $0.2V \leq V_{th} < 0.8V$.
TxBitstuffEnable	IN	Gives legacy host controllers direct control over transmit bit stuffing.
FsLsSerialMode	IN	Enables the legacy Full Speed, Low Speed Serial Mode signals.
Tx_Enable_N	IN	Active low transmit enable. FsLsSerialMode only.
Tx_DAT	IN	Transmit differential data on D+ / D- . FsLsSerialMode only.
Tx_SE0	IN	Transmit single-ended zero on D+ / D- . FsLsSerialMode only.
Rx_DP	OUT	Receive single-ended data from D+ . FsLsSerialMode only.
Rx_DM	OUT	Receive single-ended data from D- . FsLsSerialMode only.
Rx_RCV	OUT	Receive differential data from D+ / D- . FsLsSerialMode only.
<i>Level 2</i>		
XcvrSelect(1)	IN	An extra bit is added to Transceiver Select for selecting Low Speed.
<i>Level 3 (No additional signals. XcvrSelect is further encoded)</i>		
XcvrSelect(1)	IN	Transmit and receive Low Speed packets over a Full Speed bus.

Table 2 – Functional summary of UTMI+ signal additions

ULPI Overview

The ULPI specification reduces the Link to PHY interface to 12 or 8 signals, with support for all the features needed by USB peripherals, hosts, and OTG. The result is a package size of 32 pins or less, compared with 64 to 80 pins for UTMI+.

The functionality of all UTMI+ levels can be communicated through the ULPI bus. This allows transceiver chips based on the ULPI standard to be used in USB peripheral, host, and OTG applications. It is left to the Link or PHY designer to choose the level of support provided.

Interface Signals

The ULPI specification defines a bus consisting of a clock, three control signals, a bi-directional data bus, and bus arbitration. The concept is illustrated in Figure 6, and signals described in Table 3. The **dir** signal is the arbitrator of the bus.

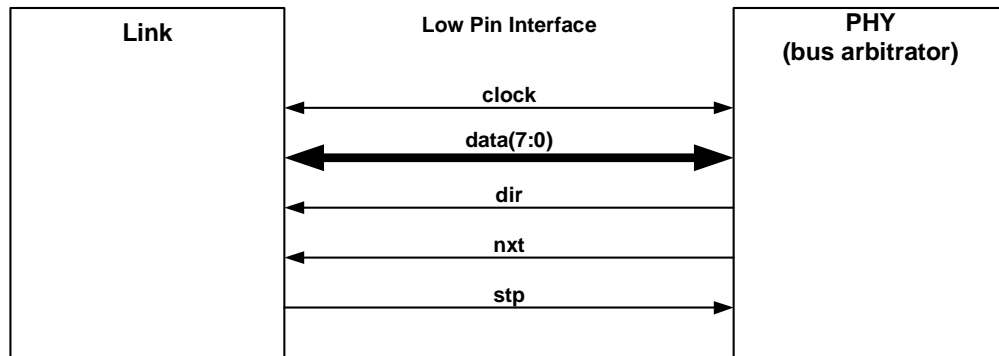


Figure 6 – ULPI signals

Name	Direction	Description
clock	I/O	Interface clock. By default, control and data signals are synchronous to clock .
data	I/O	Data bus. Driven low by the Link during idle. The Link starts a transfer by sending a non-zero pattern. The PHY must assert dir before using the data bus. A turnaround cycle is required every time that dir toggles.
dir	OUT	Direction of the data bus. By default, dir is low and the PHY listens for non-zero data from the Link. The PHY asserts dir to get control of the data bus.
nxt	OUT	Next data. The PHY drives nxt high to throttle the data bus.
stp	IN	Stop data. The Link drives stp high to signal the end of it's data stream. The Link can also drive stp high to request data bus access from the PHY.

Table 3 – ULPI interface signals

The Building Blocks of ULPI

The ULPI specification further defines interface timing, and then routes UTMI+ Level 3 through the ULPI signals. The ULPI building blocks include several features that ensure a low-pin interface while safely compressing all the UTMI+ functions and signals.

Clear Interface Timing Requirements

The ULPI specification preserves the following UTMI clock timing requirements:

- Nominal clock frequency of 60MHz. Clock is always output from the PHY.
- Clock must be within 10% of nominal frequency with a 10% duty cycle, 5.6ms after starting up. This allows a USB peripheral to wake up in time to respond to chirp signaling.
- Clock must be within 500ppm of nominal frequency with 10% duty cycle, 7ms after starting up. This allows a USB peripheral to start sending USB packets after chirp completes.

The ULPI specification adds the following requirements:

- Clock duty cycle must always be within 5% if the 4-bit data bus implementation option is used.
- Clock must startup in less than 1ms for a USB host. This allows the host to respond to remote wakeup signaling.
- The clock direction can optionally be reversed. Instead of the PHY providing a 60MHz output clock, the Link can provide the 60MHz clock as an input to the PHY. The crystal pins can be removed from the PHY, reducing the package size and removing the need for an extra crystal on the board.

Neither UTMI nor UTMI+ defines setup, hold, or output delay timing for control and data signals. Within the USB community, this has led to interoperability problems when connecting a Link chip of one vendor to a PHY chip of another vendor. The ULPI specification removes this confusion by defining timing for all interface signals.

Interface Modes

By recognizing that certain groups of signals are never used simultaneously, each group can be defined as a different mode for the ULPI interface. The data bus can be re-configured on the fly to carry new signals. The ULPI specification defines the following modes.

- Synchronous Mode (default, as defined in Table 3). This mode carries USB transmit and receive data, status bytes, and register read/write data.
- Low Power Mode.
- 6-pin FS/LS Serial Mode (optional).
- 3-pin FS/LS Serial Mode (optional). This is a compressed version of 6-pin serial mode.
- Carkit Mode (optional).

Other, vendor-specific modes can also be defined.

Bi-directional Data Bus

The ULPI data bus is bi-directional and carries many different data types. The PHY unconditionally gains ownership of the data bus by asserting **dir**, as shown in Figure 7. A turnaround cycle is required whenever the bus changes direction.

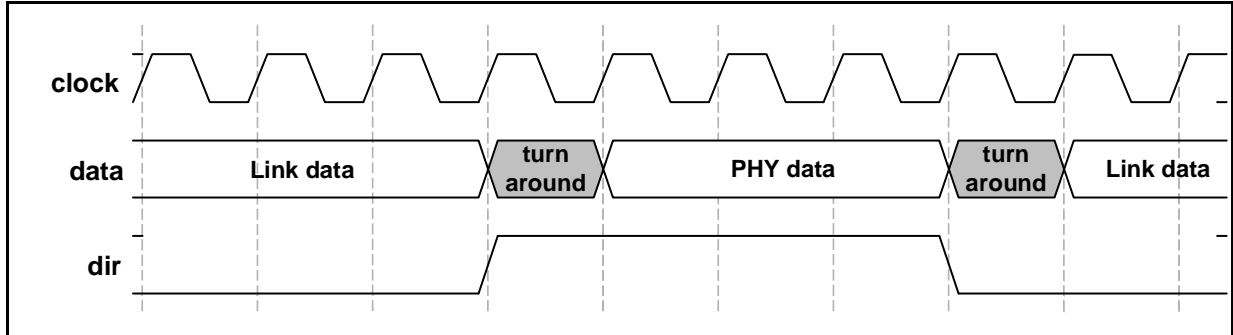


Figure 7 – ULPI data bus ownership and turnaround cycles

Double Data Rate Bus

A standard implementation of ULPI uses an 8-bit data bus. An optional 4-bit data bus that operates at double data rate is also defined. The least significant 4 bits of a data byte are transmitted first on the rising clock edge. The most significant 4 bits are then transmitted on the falling clock edge.

This feature does not exist in UTMI or UTMI+. It was included in ULPI to reduce the number of interface signals from 12 to 8.

Note that because USB data is always byte-aligned, clocking control signals at double data rate is neither necessary nor allowed.

Reuse of Control Signals

The **dir**, **stp**, and **nxt** control signals are reused to control various aspects of each interface mode. Table 1 summarizes how control signals are used in each mode.

Mode	dir	stp	nxt
Synchronous	Data bus direction and packet framing	End of transmit packet	Accept/request next byte
Low Power	Always asserted	Wake up the PHY	Not used
Serial	Always asserted	Exit serial mode	Not used
Carkit	Always asserted	Exit carkit mode	Not used

Table 4 – Function of dir, stp, and nxt in each interface mode

PHY Register Set

A set of registers, defined in the PHY, stores various settings and status information. All register operations have a lower priority than USB transmit and receive data. The registers contain many UTMI+ signals that have been chosen carefully to ensure they are not timing critical, nor are they required to be changed during USB data.

Note that UTMI+ does not define any registers, so this is a new concept that may impact current IP performance. The designer should carefully analyze IP requirements before converting a UTMI+ IP into a ULPI compliant part.

There are four main types of registers:

- | | |
|----------------------------|--|
| ID Registers | These registers provide a unique identifier to the USB system. If necessary, system software can change behavior based on different PHY attachment. This is not generally needed because PHY capabilities are chosen at hardware design time. |
| Mode Registers | These registers control how the PHY behaves. Many signals from UTMI+ are changed only when the USB is idle, so they are placed in registers that are accessed only when the ULPI bus is idle. Several new features have also been introduced, including Carkit Mode. |
| Interrupt Registers | These registers inform the Link of status changes in the PHY. Many signals in UTMI+ convey information to the Link that is not timing critical. Those signals have been replaced with status bytes and interrupt signaling. Status information is sent only when the ULPI bus is idle. |
| Extra Registers | Additional register space is provided for two reasons. Some addresses have been reserved for future use, while other registers are available for vendor-specific use. |

Other Features

- The first byte transmitted by the Link in Synchronous Mode is called the Transmit Command Byte, or TX CMD. Normally a PID byte, it is overloaded in ULPI with register read and write commands.
- Full bus arbitration. The PHY can gain control of the bus at any time by asserting **dir**. If the PHY owns the bus, the Link can assert **stp** to temporarily regain control of the bus.

ULPI Design Implications

Listed here are some of the more important design implications that have arisen due to the new features introduced by ULPI.

ULPI as a Wrapper around UTMI+

Since the goal of ULPI is to reduce the number of interface pins while enabling reuse of existing IP, the specification focuses on converting the UTMI+ interface to ULPI by using a simple wrapper.

The wrapper concept is illustrated in Figure 8. If any wrapper contains flip-flops on signals such as TXValid, TXReady, RXActive, RXValid, or LineState, this will introduce extra cycle(s) of delay. Such delays will impact the time budgeted for USB turnaround and Link Decision Time. It is recommended that the designer re-optimize the UTMI+ core timing to gain back the extra cycle(s).

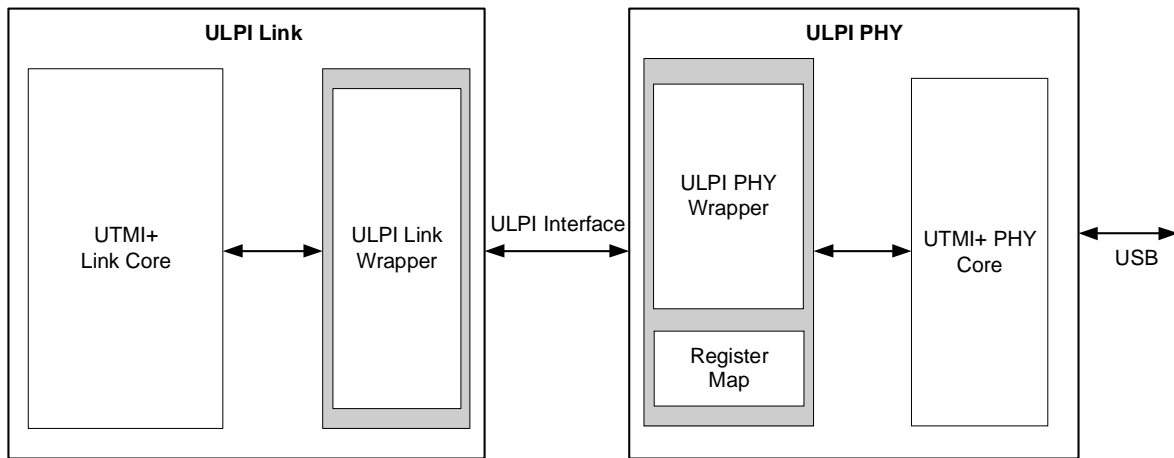


Figure 8 – Creating a ULPI system using wrappers around UTMI+

Faster Clock Startup Time For Hosts

If a USB host receives wakeup (resume) signaling from a peripheral, the host must repeat the resume signaling on the same port within 1ms. To transmit the resume signaling, the host will have to wake up its clock. In UTMI, the clock startup time is defined as 5.6ms, which is too slow to meet the 1ms resume timing specification. Hence, ULPI recommends a clock startup time of less than 1ms. However, if the 1ms clock startup requirement cannot be met, for whatever reason, the PHY must internally transmit the resume signaling without the presence of the clock.

Data Bus Direction Control

In UTMI+, the Link controls the direction of the data bus by asserting TXValid. In ULPI, this mechanism is reversed. In the link, the **dir** signal can be used to directly control the bi-directional I/O buffers on the chip pins. In the PHY, a clocked version of **dir** can be used to control the I/O buffers.

Clock Suspend

ULPI introduces a new mode register to control power to the clock circuitry. The designer should take care to ensure that the clock powers down without glitches.

The clock can be powered down in Low Power Mode, Serial Modes, and CarKit Mode. When the clock is powered down, the Link and PHY must drive signals combinatorially.

- In Low Power Mode, LineState must be driven directly from the Full Speed analog receivers. The interrupt pin must only be asserted when a new interrupt occurs.
- In Serial Mode, the Link must always drive the transmit pins. The PHY must drive the receive pins and assert the interrupt pin only when a new interrupt occurs.
- In CarKit Mode, the UART TXD/RXD must be driven directly by analog circuits. The interrupt pin must only be asserted when a new interrupt occurs. This must be detectable without a clock present.

Circuits Required for UTMI+ Levels

A peripheral PHY based on UTMI+ Level 0 requires Full Speed and High Speed analog transceivers with non-trivial digital logic for serializing, de-serializing etc.

A host PHY based on UTMI+ Level 1 requires extra digital logic for detecting when a peripheral is connected or disconnected.

An OTG PHY based on UTMI+ Level 1 requires various VBUS voltage comparators, VBUS charge/discharge circuitry for SRP, and optionally a charge pump for driving VBUS. A circuit is required to detect which end of the cable is plugged in.

A host or OTG PHY based on UTMI+ Level 2 requires extra digital logic for Low Speed packet processing, as well as a Low Speed analog transceiver.

A host or OTG PHY based on UTMI+ Level 3 requires extra digital logic to automatically wrap packets with a Full Speed preamble header.

Carkit Option

Cell phones are moving to adopt a single USB connector as their primary physical interface. This connector will be used to connect to PC's and other USB devices, and will also be used to connect to car stereos. An example of this is shown in Figure 9. Connecting a phone to a car stereo allows the car stereo to be used as a speakerphone. This allows hands free operation of the phone.

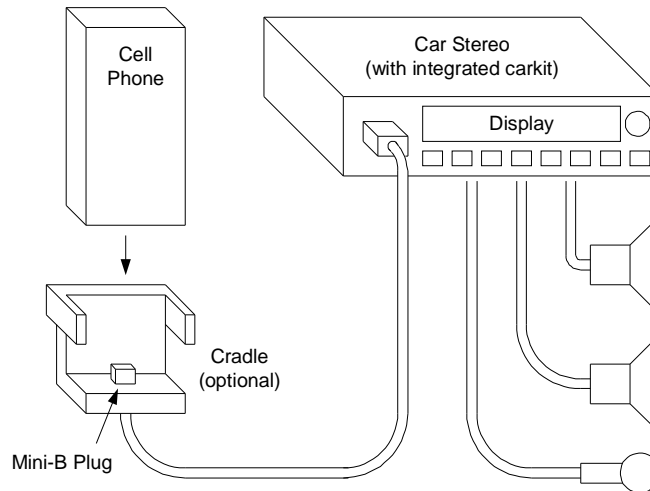


Figure 9 – Cell phone hands free operation

ULPI specifies an optional carkit mode. When a cell phone is initially connected to a carkit, the phone and carkit enter a UART signaling mode. This allows the phone to discover what features the carkit has, and enable or disable them as appropriate. The phone and carkit then enter an audio signaling mode, where the D+ and D- lines are used for analog signaling. The basic architecture of the interface, and the allowed signaling modes, are shown in Figure 10.

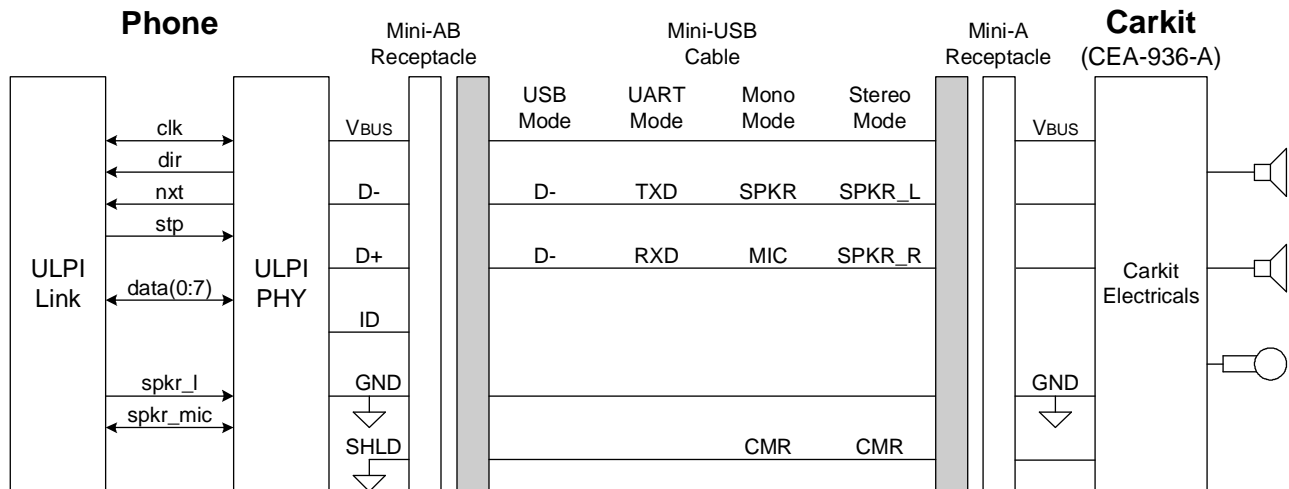


Figure 10 – Carkit interface

It must be noted that the carkit specification (CEA-936-A) is now obsolete. However, various features of carkit mode are useful for other purposes. For example, the register used to enable audio bypass is useful for analog headset applications.

Interoperability Testing

ULPI defines a standard connector that allows multi-vendor link and PHY cards to seamlessly connect for testing purposes. A daughter-card containing a ULPI PHY IC is defined with dimensions given by the original T&MT specification for UTMI. The connector pin assignment is detailed in the ULPI specification.

An example daughter-card and PCI-based Link board is depicted in Figure 11. It is important to note the orientation of the 100-pin Amp connector and the USB receptacle.

The ULPI T&MT interface has the following features:

- 100 pin Amp connector.
- Compatible with UTMI and UTMI+ T&MT connector pin assignments where possible.
- Routes all ULPI digital interface pins between Link and PHY.
- Provides 15 general-purpose I/O pins for vendor-specific functions.
- Multiple power and ground pins.
- Switchable V_{BUS} power control.
- Defines separate I/O voltage pins with vendor-specific I/O voltage levels.

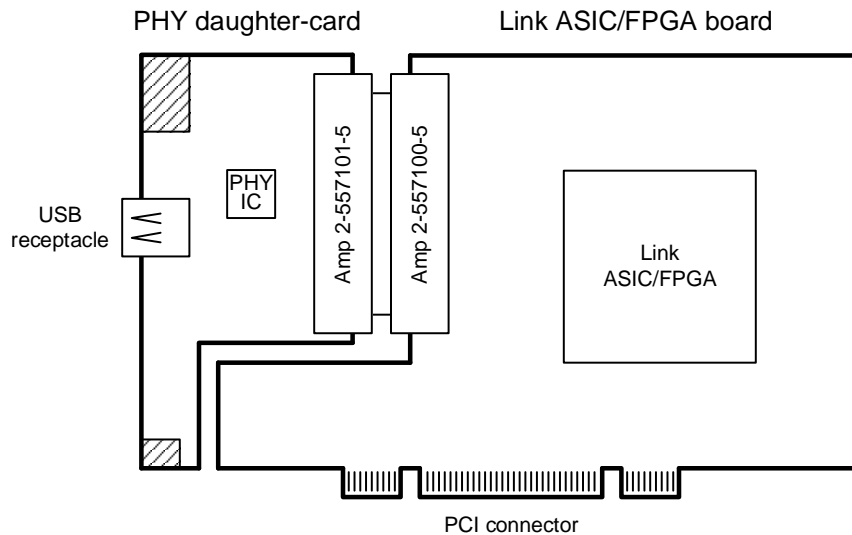


Figure 11 – Recommended T&MT board configuration (not to scale)

ULPI Promoter Companies

The following companies promoted and contributed to the development of the ULPI Specification.

- ARC International Inc.
- Conexant Systems, Inc.
- Mentor Graphics Corporation
- SMSC
- ST-Ericsson
- TransDimension, Inc.

Contact Information

The ULPI specification can be found at <http://www.ulpi.org>.

For further inquiries, email to info@ulpi.org.